Design of Low Power ALU Operations using m-GDITechnique

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Abstract -. The ALU is constructed from modular blocks like full adder and full subtractor for arithmetic operations and logic gates for bitwise operations. These blocks are designed using m-GDI cells, leading to a more compact and power-efficient implementation. The ALU also incorporates a multiplexer to select between the arithmetic and logic outputs based on the control signal. The design prioritizes minimizing transistor count and maintaining low power consumption while ensuring accurate and efficient ALU operation. This work contributes to the development of low-power and compact digital circuits. The m-GDI based ALU offers a promising alternative to traditional CMOS designs for resource-constrained applications in embedded systems and portable devices. Further research can involve performance analysis through simulations and comparisons with existing ALU designs to solidify the efficiency gains achieved through the m-GDI approach. The result will be simulated by using DSCH-3.1 and MICROWIND 3.1.

Index Terms - ALU, m-GDI, VLSI Design, Full Adder, Full Subtractor, DSCH 3.5, Verilog, Micro wind 3.1.

I. INTRODUCTION

VLSI stands for Very Large Scale Integration, and it refers to the method of building integrated circuits (ICs) by merging thousands to millions of transistors on a single chip. VLSI technology has been crucial in the progress of modern electronics, allowing for the creation of powerful and compact electronic devices such as microprocessors, memory chips, and digital signal processors.GDI (Gate Diffusion Input) is a new technique for designing low-power digital circuits. This approach reduces the power consumption, latency, and size of digital circuits while keeping the logic simple. Gate Diffusion Input, or GDI, is a revolutionary circuit design technique that significantly reduces power needs.Modified Gate Diffusion Input (MGDI) is a technique used in the design of digital integrated circuits, particularly in CMOS (Complementary Metal- Oxide-Semiconductor) technology. It is a variation of the conventional gate diffusion input technique used in CMOS logic circuits. In CMOS technology, the gate diffusion input structure is a common way to implement logic gates. In this structure, the gate of a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) is connected directly to the input signal. However, in the case of MGDI, there are modifications made to this conventional structure to enhance the performance of the circuit. The main part of a Central Processing Unit (CPU) is the Arithmetic Logic Unit (ALU).It is responsible for performing arithmetic and logic operations on binary data. It is a key building block for executing arithmetic calculations, logical comparisons, and bitwise operations in a computer system. NOT gate, also known as an inverter, is a fundamental logic gate that performs the logical operation of negation It takes an input signal and produces an output signal that is the complement of the input signal. In other words, if the input is high (logic 1), the output is low (logic 0), and vice versa.The AND gate is a fundamental logic gate that implements the logical AND operation. . It takes two or more input signals and outputs a single signal. The output is high (logic 1) only when all input signals are high; otherwise, the output is low (logic 0).The OR gate is a fundamental logic gate that conducts logical OR operations. It accepts two or more input signals and outputs a single signal. The output is high (logic 1) if any of the input signals is high; otherwise, the output is low (logic 0).NAND gate is a fundamental logic gate that performs the logical NAND (NOT-AND) operation. It takes two or more input signals and outputs a single signal. A NAND gate's output is the inverse of the logical AND operation; it is high (logic 1) if any of the input signals are low (logic 0).NOR gate is a fundamental logic gate that performs the logical NOR (NOT- OR) operation. It combines two or more input signals to form a single output signal.. The output of a NOR gate is the inverseof the logical OR operation; it is high (logic 1) if all input signals are low (logic 0); otherwise, the output is low (logic 0).The XOR gate (Exclusive OR gate) is a basic logic gate that executes the logical XOR operation. It has two input signals and produces a single output signal. The output is

high (logic 1) if the two input signals are different; otherwise, the output is low (logic 0).XNOR gate (Exclusive NOR gate) is a fundamental logic gate that performs the logical XNOR operation. It has two input signals and produces a single output signal. The output is high (logic 1) if the two input signals are the same (both high or both low); otherwise, the output is low (logic 0).A full adder is a combinational logic circuit that adds three input bits: A, B, and a carry-in (Cin), resulting in a sum (S) and a carry-out. It essentially adds two single-bit binary numbers along with a carry from a previous addition .Full subtractor is a combinational logic circuit that subtracts two single-bit binary numbers along with a borrow from a previous subtraction. It takes three input bits: A, B (minuend and subtrahend, respectively), and aborrow-in (Bin), and produces a difference (D) and a borrow-out (Bout).Comparator is a combinational logic circuit used to compare two binary numbers or digital signals and determine their relative magnitudes. The output of a comparator indicates whether one input is greater than, less than, or equal to the other input.

II. EXISTING METHOD

Using M-GDI the XOR gate can be implemented by employing only three transistors(Using GDI it take 4 transistors).The biggest problem in GDI is the difficulty in fabrication using CMOS .In the modified GDI cell the bulk terminals of PMOS and NMOS connected to VDD and Ground respectively. We incorporate a mechanism that would enable us to choose any one from all the logical and arithmetic modules. For this, taken a 1-to-8 demultiplexer which will work in tandem with sixteen sleep transistors (2 for each module) to choose and enable the desired circuitry. XOR Adder and 8T SUBTRACTOR using m-GDI.OR, NOT, NAND, AND and 3T XOR using m-GDI.

1.OR m-GDI

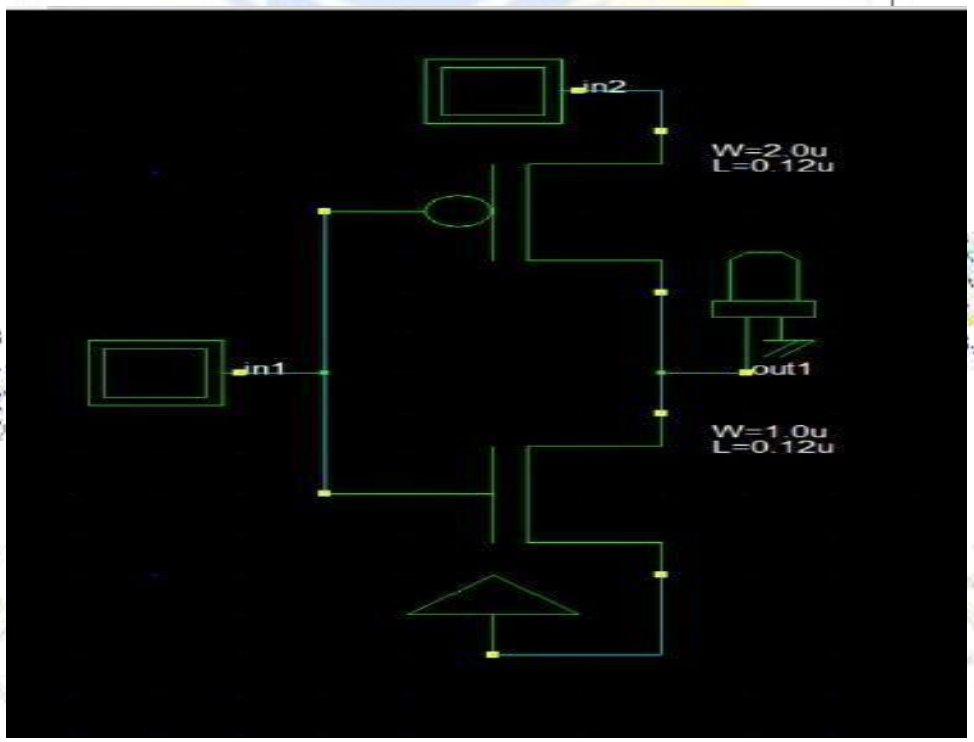

Fig.1:OR m-GDI

2.NOT m-GDI

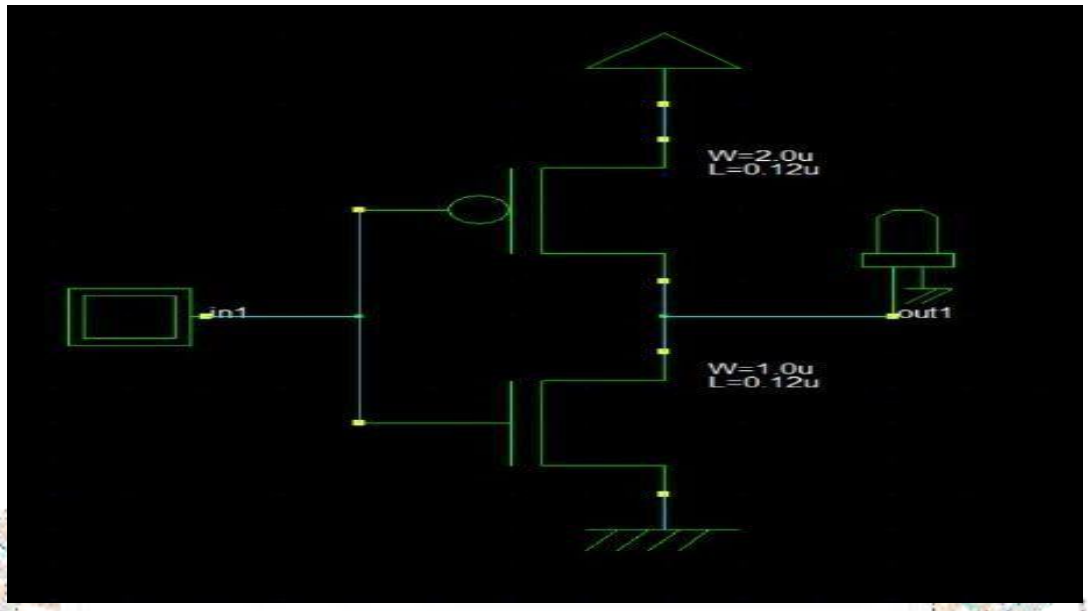

Fig.2:NOT m-GDI

3.NAND m-GDI

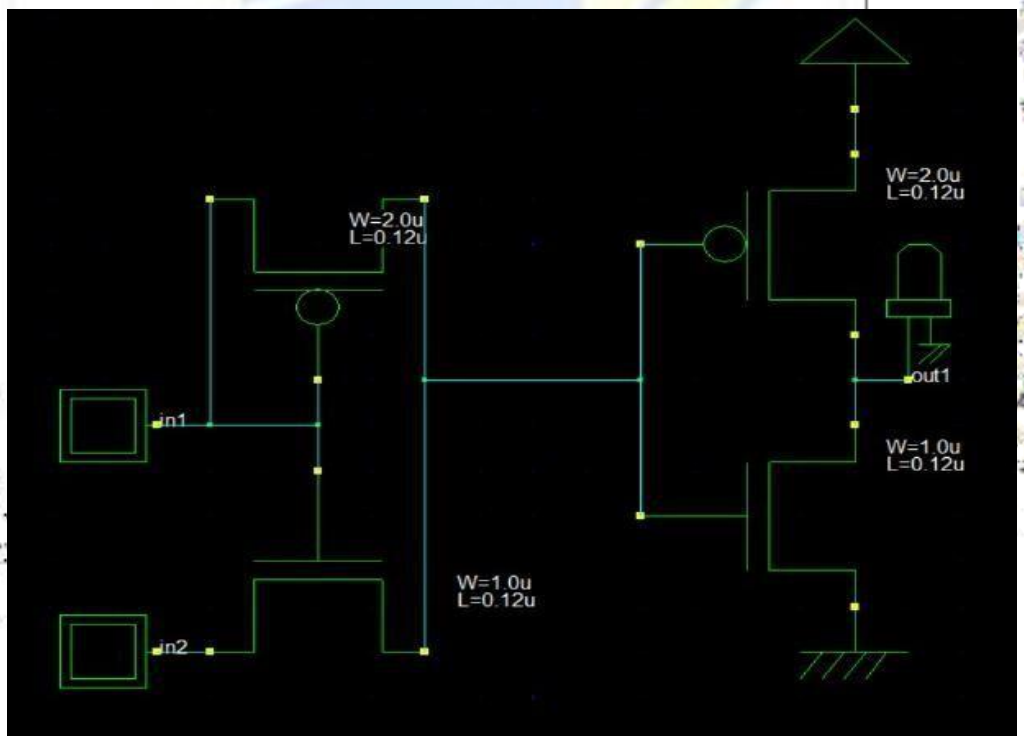

Fig.3:NAND m-GDI

4.AND m-GDI

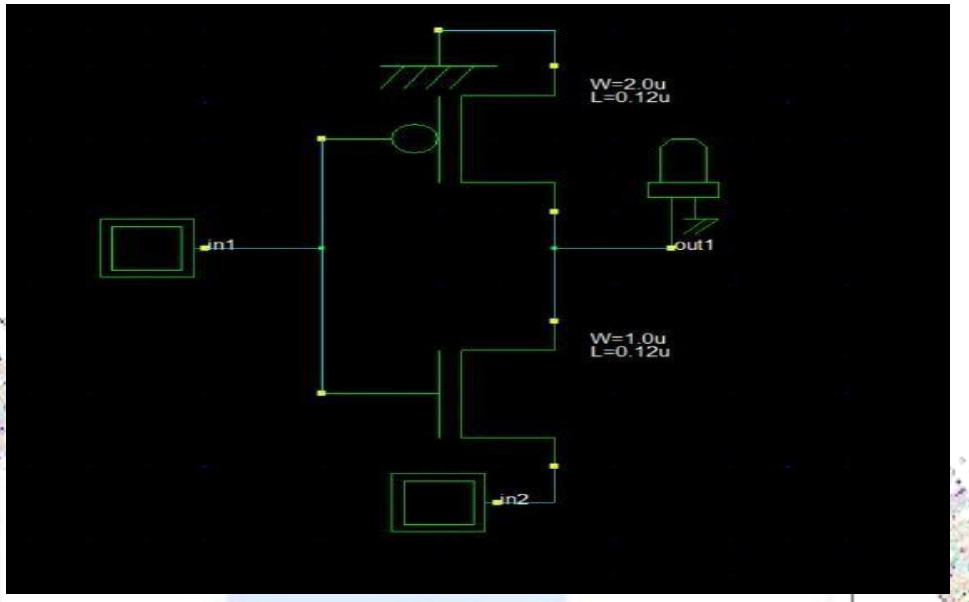

Fig.4:AND m-GDI

5. 3T XOR (m-GDI)

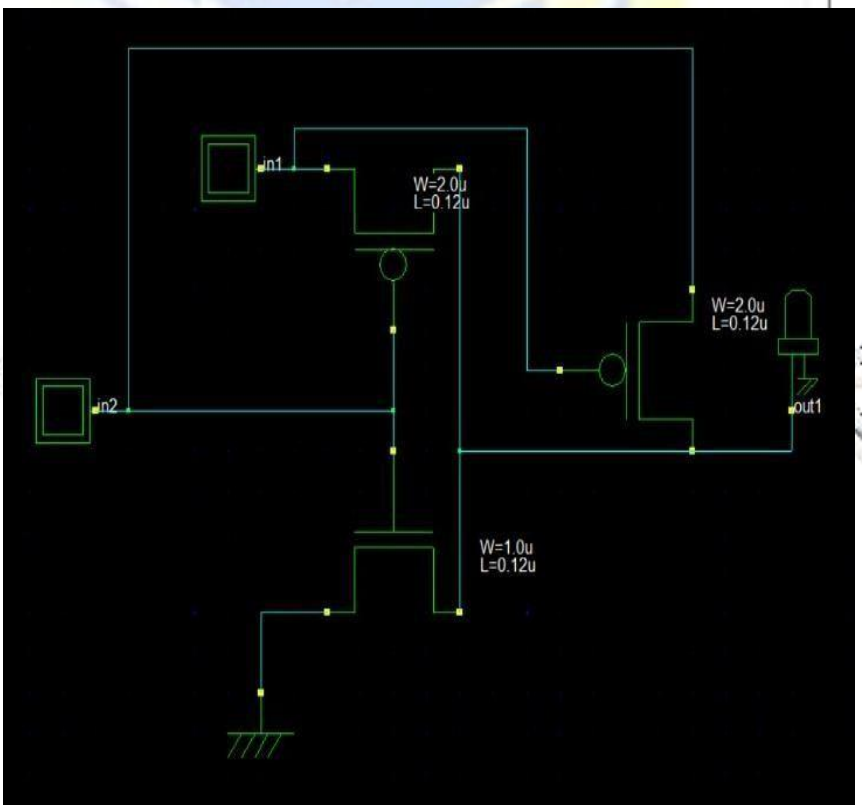

Fig.5:3T XOR m-GDI

6. XOR ADDER (m-GDI)

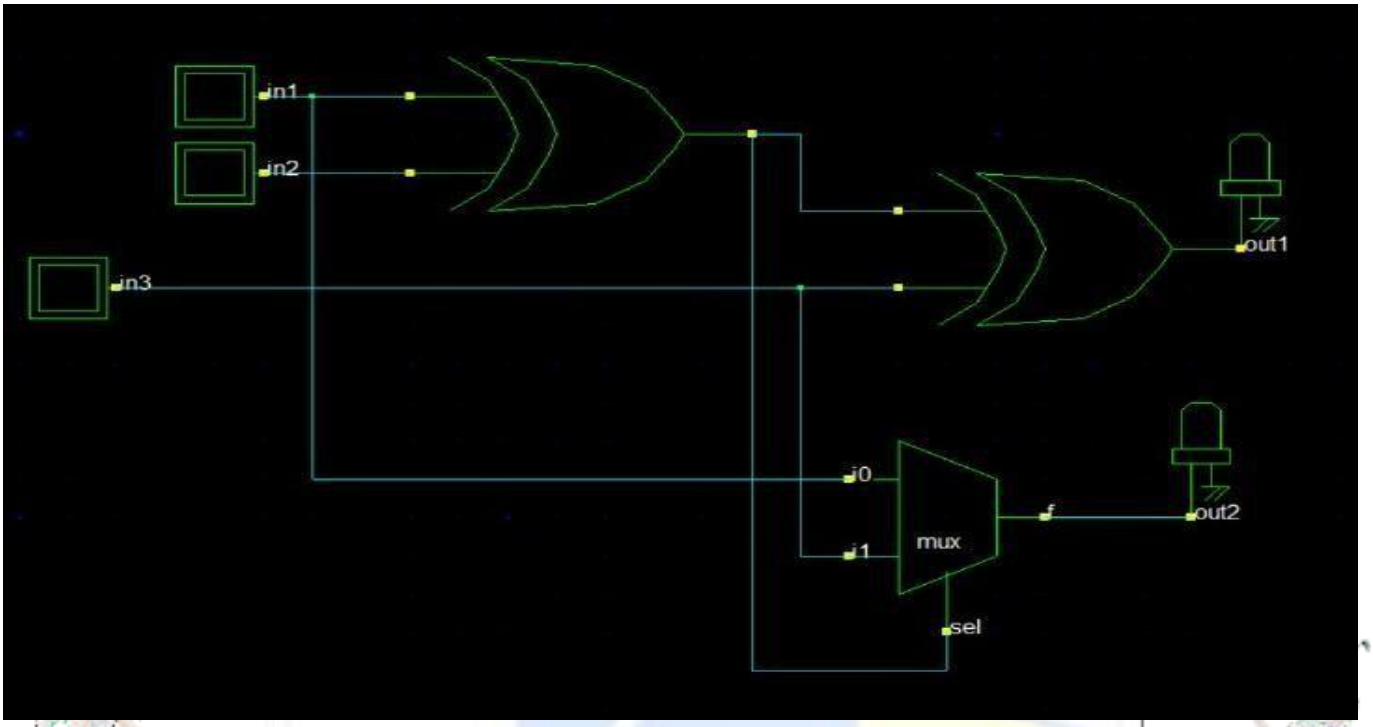

Fig.6:XOR ADDER m-GDI

7. FULL SUBTRACTOR (m-GDI)

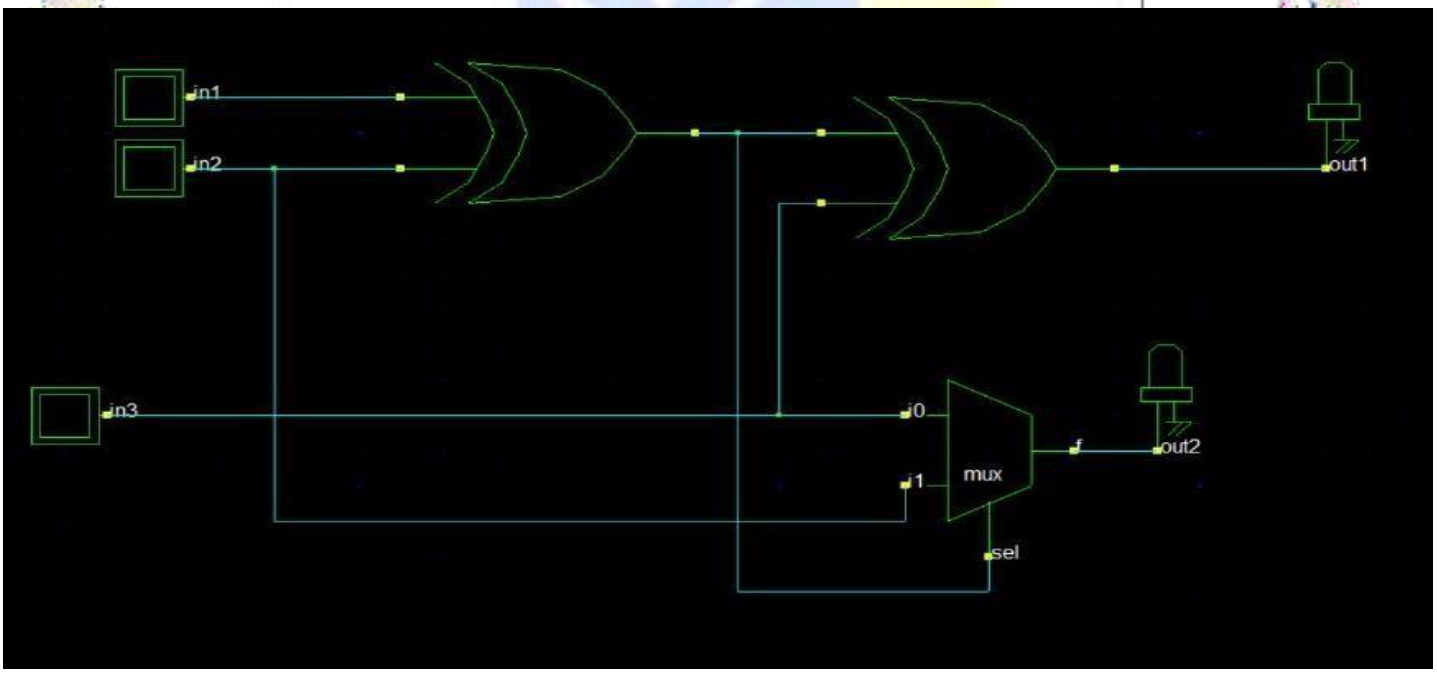

Fig.7:FULL SUBTRACTOR

8. 1-to-8 DEMULTIPLEXER USING m-GDI

Here we used the demultiplexer to designed the 1-to-8 Demultiplexer using m-GDI. And here we used only 8 operations.

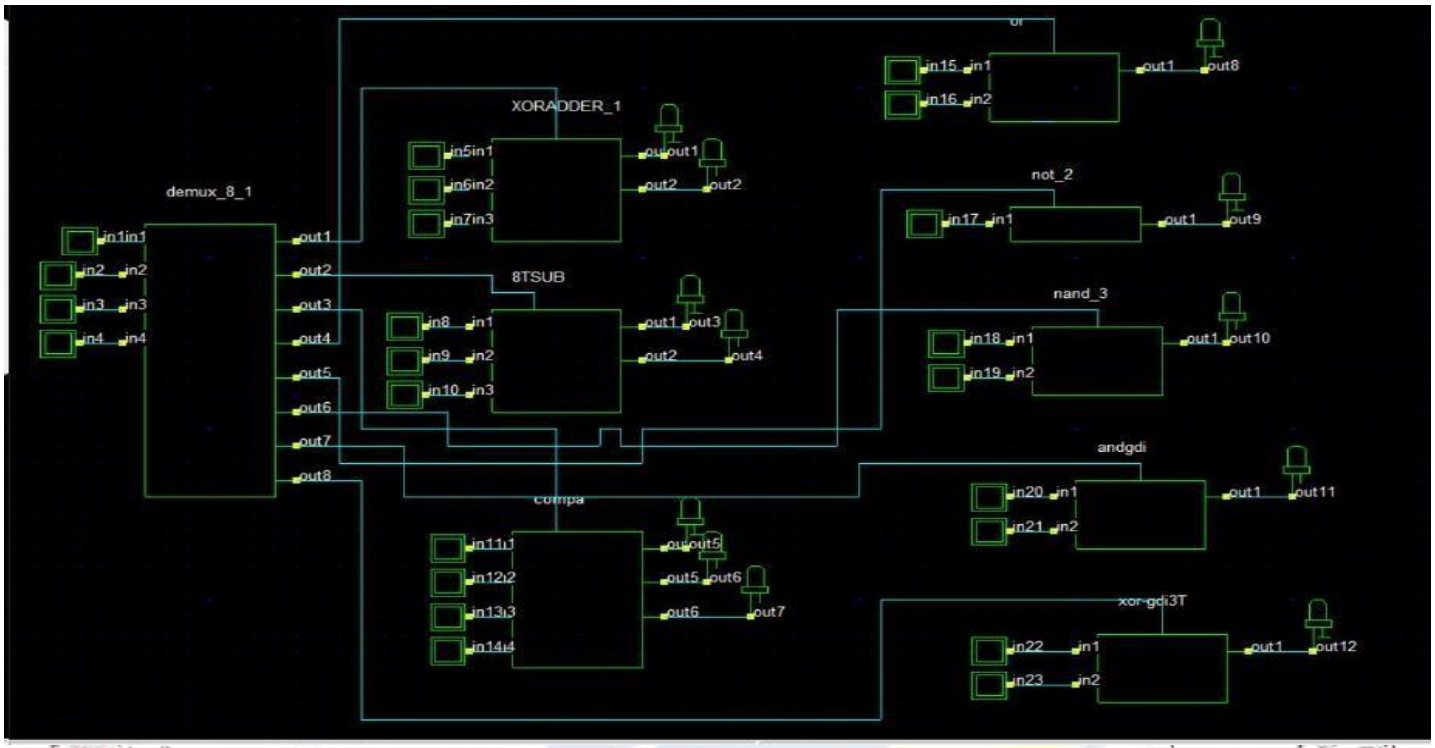

Fig.8: 1-to-8 DEMULTIPLEXER

9.SIMULATION OF 1-to-8 DEMULTIPLEXER

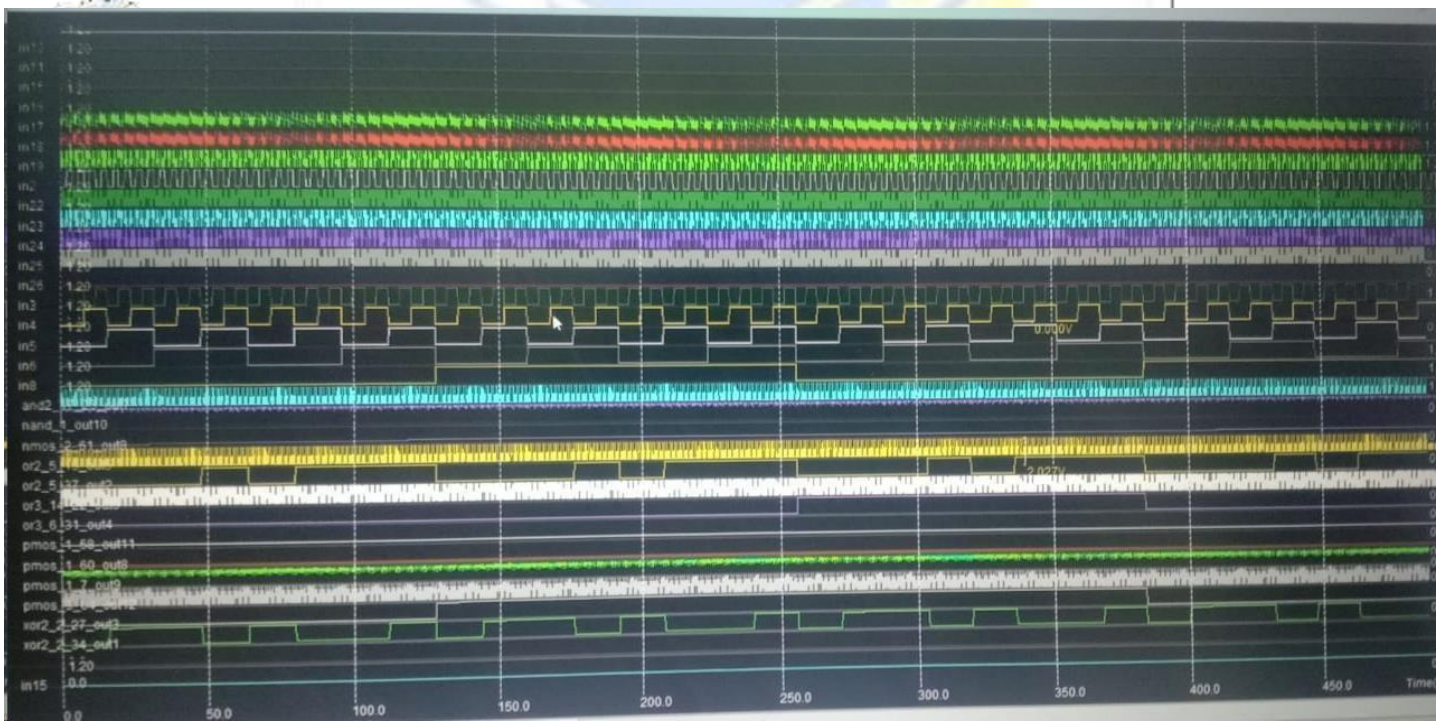

Fig.9: Simulation of 1-to-8 Demultiplexer

III. PROPOSED METHOD

In Proposed method, we are using ALU Operations i.e BUFFER, NOT, AND, OR, NAND, NOR , XOR, XNOR, FULL ADDER, FULL SUBTRACTOR,COMPARATOR, and two functions i.e F1 and F2. And here we are using the four selection lines i.e S0,S1,S2,S3 and the inputs we are considering as A,B,Cin. In the 16-bit ALU we are using 16X1 MUX. Based on the input and selection input we have given , the corresponding output will be generated. Here F1 function performs AND operation and F2 function performs OR operation as well. Here the BUFFER output will be generated according to the input of A. In this we reduced the transistors count.

1.1 ALU Operations Using MUX

Here we are using 16X1 multiplexer to design the 16-bit ALU.A, B, Cin are the inputs.S0,S1,S2,S3 are the selection lines. We are using BUFFER,NOT,AND,OR,NAND,NOR,XOR,XNOR,FULLADDER,FULLSUBTRACTOR,COMPARATOR,F1 F2 are the two functions used to perform ALU.operations..

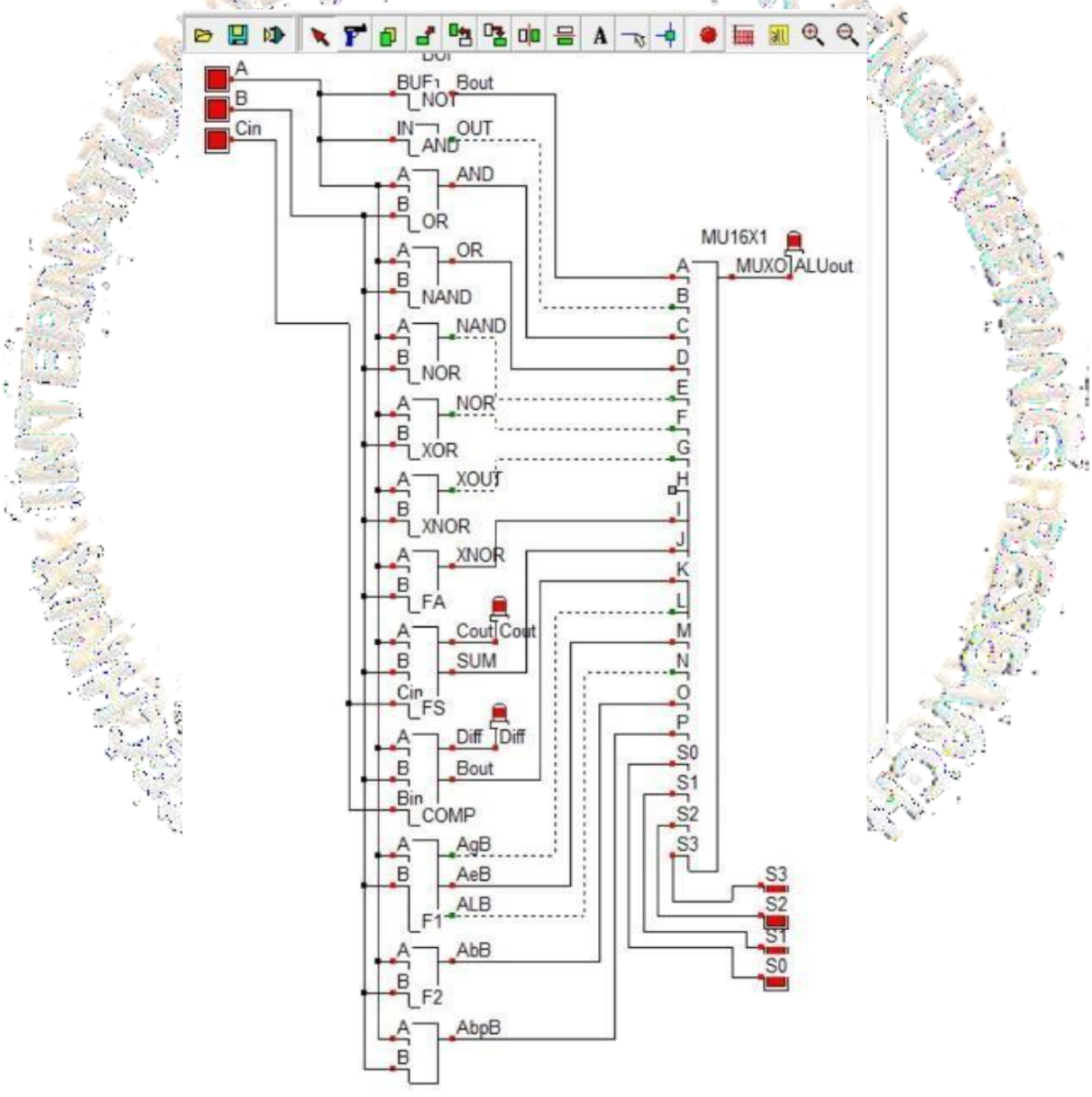

Fig.10:ALU Operations

2.Simulation of ALU Operations

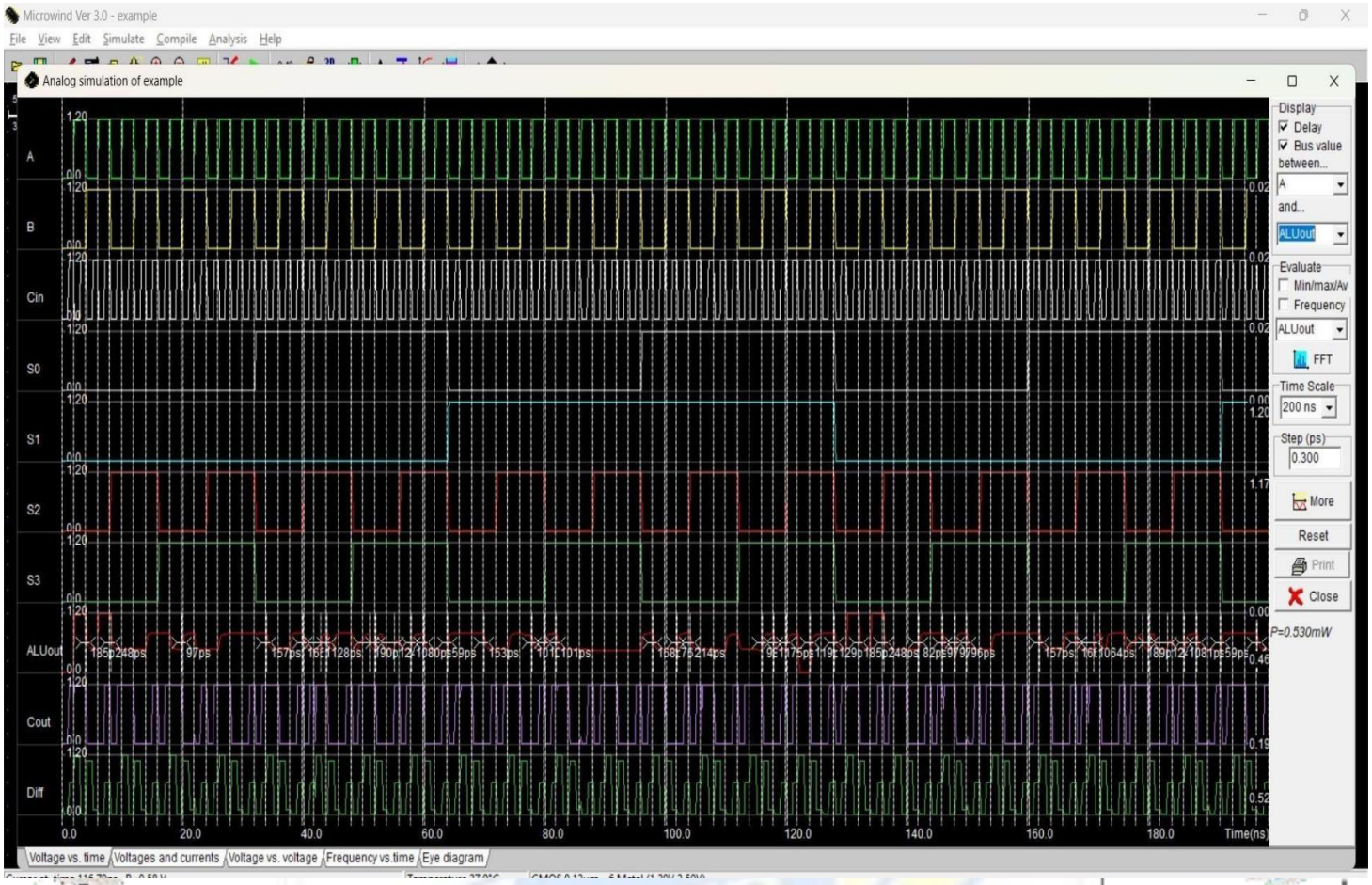

Fig.11:Simulation of ALU Operations

IV. CONCLUSIONS

Compared to 1-to-8 Demultiplexer the number of transistor count is reduced in the ALU Operations. And in the ALU Operations we used the multiplexer.

V. REFERENCES

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